REMARKS

The examiner rejected claims 1-6 and 8-11 and allowed claim 7. Claim 8 was rejected under 35 U.S.C. §102(e) as being anticipated by US patent 6,747,695 to Afghahi. The remaining claims were rejected under 35 U.S.C. §103(a) as being unpatentable over US patent 4,996,413 to McDaniel et al. or US patent 6,366,320 to Nair et al. or US patent 5,965,871 to Zhou et al. or a combination thereof.

SUMMARY OF RESPONSE

In response, applicant has canceled claims 2, 6, 8, 9 and 11, and amended claims 1, 3-5, 7 and 10. Applicant's amended claims relate to the use of a plurality, i.e., two or more multiplexed column buffers. In applicant's specification, a multiplexed column buffer is that portion of the output signal processing that is repeated on a per multiple column basis, i.e., repeated for every group of columns in the array of active pixel sensors (APS). For example, an active pixel sensor array with 1280 columns, using a column buffer that multiplexed 2 columns per column buffer, would have 640 such multiplexed column buffers. Similarly, if the column buffer multiplexed 4 columns, the chip would have 320 substantially similar multiplexed column buffers.

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The problem of pattern noise in an active pixel sensor array is well known. Removal of pattern noise by subtracting the active pixel sensor reset value from the active pixel sensor signal value is sometimes called correlated double sampling (CDS).

The "column buffers" in cited patents to Nair et al., Zhou et al. and Afghahi show two memory elements per column (i.e., memory for storing pixel signal and pixel reset values per column). The subtraction of pixel reset value from pixel signal value is not repeated on a per column basis. Instead, the subtraction function (like the MUX and bus amplifier functions) is provided once for the whole chip, and is not provided on per column nor on a per group of columns basis. Applicant's amended claims distinguish Nair et al., Zhou et al., Afghahi and McDaniel et al. by reciting two or more multiplexed column buffers, where each such multiplexed column buffer is able to multiplex two columns and includes structure for the cancellation of pattern noise in each of such multiplexed column buffers.

THE CITED PRIOR ART

US patent 6,366,320 to Nair et al.

Nair et al. repeat a "sense amp cell" 116 (one per column) in figures 1 and 2. Nair et al. show a pair of sample/hold memories C_{SA1}, C_{SA2} with a pair of current amplifiers A1, A2 on a per column basis, producing one pair of current signals per column. On a per chip basis, an analog MUX 118 selects a pair of current signals that are thereafter CDS processed (by subtraction) and the result sent to an analog output amplifier.

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US patent 5,965,871 to Zhou et al.

Zhou et al. repeat a "readout circuit" 22 (one per column) in figure 1. Zhou et al. show a show a pair of sample/hold memories 26, 27 with a pair of voltage amplifiers 29, 30 on per column basis, producing one pair of voltage signals per column. On a per chip basis, column decoder 21 selects a pair of voltage signals for each column that is thereafter CDS processed (by subtraction) by an analog output amplifier 25. Zhou et al's approach is similar to Nair et al's, except for using voltage mode in lieu of current mode.

US patent 6,747,695 to Afghahi

Afghahi repeats a CDS cell 135 (one per column) in figure 1. Each cell 135 has a pair of sample/hold memories with a pair of current amplifiers (sample path and calibration path). On a per chip basis, the analog MUX 140 selects a pair of current signals 580 in figure 5, which is thereafter CDS processed (by subtraction) in DDSSB6 in figure 6. Afghahi shows the same approach to column buffer design, as do Nair et al. and Zhou et al.

US patent 4,996,413 to McDaniel et al.

McDaniel et al. show an entirely different application for image sensor readout circuits. McDaniel et al. show a method for reading data from an image detector array, which image detector has a greater resolution than is necessary for the particular application (X-ray imaging). To reduce the resolution of the image detector array, McDaniel et al. select a group of adjacent pixels and take the average value of the group if pixels. In figures 4 and 5, adjacent pixels in columns 1, 2, 3 and 4 are selected by an analog MUX A, MUX B, MUX C and MUX D and added together (in adder 64 in figure 4 or in amplifier 78 in figure 5).

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McDaniel et al's column buffer does not read out each column value, nor does it cancel pattern noise by the use of correlated double sampling (CDS).

DISTINGUISHING THE PRIOR ART

Thus, the "column buffers" shown by 116 in Nair et al., 22 in Zhou et al. and 135 in Afghahi consist of the two memory elements that hold pixel signal and pixel reset values, and the two current or voltage buffers, one for each memory element. The remainder of the column signal's processing, i.e., the MUX column selection, the CDS subtraction (signal value minus reset value) and the bus amplifier are not repeated on a group of column basis. Instead, in any of Nair et al., Zhou et al. or Afghahi, the MUX, CDS and bus amplifier are not repeated at all, but are presented once on a per chip basis, i.e., once per chip (one MUX, one CDS and one bus amplifier for all the columns on the chip).

THE AMENDED CLAIMS

Claim 7 has been allowed. Applicant has amended claim 7 to correct minor errors without changing the substance of the claim. Allowance of claim 7, as amended, is requested.

Amended claims 1 and 3-5 recite a "plurality of multiplexed column buffers" not shown by Nair et al., Zhou et al. or Afghahi. Claim 10 recites first and second "multiplexed column buffers." Amended claims 1, 3-5 and 10 also recite structure for accomplishing pattern noise cancellation (CDS) in an active pixel sensor array on a semiconductor chip.

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For example, claims 1 and 3-5 recite "first, second, third and fourth memory elements...." Claim 10 recites "a first corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value," and "a second pattern cancellation circuit for providing a second corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value," where the first and second "multiplexed column buffers" ultimately provide a "sequential[ly] readout [of] corrected APS pixel signal values for said first, second, third and fourth columns of said array of active pixel sensors at said output terminal."

Since Nair et al., Zhou et al. or Afghahi show one pattern noise cancellation (CDS) for the whole chip, in addition to MUX and bus drivers for the whole chip, it would not be obvious to use a "plurality" of such elements and multiplex such plurality of multiplexed column buffers on a group of columns basis. Nor do McDaniel et al. (who do not use CDS or readout multiplexed column data) add to the disclosure of Nair et al., Zhou et al. or Afghahi to render the amended claims obvious.

CONCLUSION

Applicant has made an earnest effort to present claims patentably distinct from the references, and point out how the specific language of the claims patentably distinguishes such references.

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For the reasons given above, applicant submits that claims 1, 3-5, 7 and 10 as amended are not shown or suggested by Nair et al., Zhou et al., Afghahi or McDaniels et al., or any combination of them. Applicant requests that the examiner withdraw the rejection of claims under 35 U.S.C §102 and 35 U.S.C. §103, and pass the present application to issue.

Respectfully submitted,
by

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